Effect of radiation and endurance on pulsed programming of commercial NAND Flash memory

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***Abstract*—Independent and coupled effects of radiation and endurance on commercial NAND Flash memory is studied using pulsed programming enabled by interrupting the programming command at the chip-level. The effects of total ionization dose (TID) and endurance stress increase and decrease, respectively, the number of pulses needed to program an entire page. The coupled effect of endurance stress and TID appear to exhibit linear correlation. A neutral electron/ hole trap model is evaluated and correlates well with our results.**

Keywords—Radiation effects, CMOS, flash memory, endurance.

I. INTRODUCTION

Spacecraft systems use NAND Flash memory to store various mission data [1]. Outer space and deep space environments can deteriorate the performance of flash memory and lead to eventual failure [2]. Thus, understanding flash memory failures in space environments is essential for successful space missions. The failure mechanisms of flash memory components can be from the support circuitry-level or memory bit-level failure. However, information available from traditional part level failure testing is often limited due to the various possible failure mechanisms. For example, the support circuitry may fail way ahead of the actual bit failure [2, 3], thus masking any information related to possible bit-level failure. A technique which is applicable at component level while providing insights into bit level failure, is thus necessary. One such technique is partial page programming of flash memory, used by Roach et al. to study the effect of radiation and endurance [4, 5, 6]. A program operation executes for a predefined amount time, referred here as the pulse-width, resulting in a partial or pulsed program operation. The pulse-width used here is much less than the total time required to program the entire page. Therefore, the pulse-width determines the population of programmed bits during a single partial or pulsed program operation. A larger pulse-width can successfully program a larger population of bits on a page. Repeating the pulsed program operation many times will eventually program the entire page.

At the bit device level, during a program operation, the control gate is at a large positive bias [14], enabling electrons to tunnel through the tunnel oxide into the floating gate from the substrate based on the Fowler-Nordheim tunneling mechanism. In an erase operation, the control gate is under large negative bias and the electrons tunnel out of the floating gate through the tunnel oxide. The program and erase operations, when repeated many times, can lead to electrons trapped in the tunnel oxide and/or silicon-oxide interface and shift the threshold voltage to a higher value. These trapped electrons from the program-erase endurance stress can shift the threshold voltage resulting in faster programming and slower erase speed, respectively [4, 7, 23, 24, 25].

In a radiation environment with Co^{60} gamma radiation, the gamma rays create electron-hole pairs in the oxide. Since the electron mobility is much higher than hole in SiO2, under an external positive gate bias, the electron will travel to the gate electrode very much faster than hole [7, 31]. Transport of the hole is through hopping mechanism and the hole may form a trap in the tunnel oxide or may eventually arrive near the interface of the SiO_2/Si to form a trap state [5]. The positive trap state in the tunnel oxide shifts the threshold voltage of the memory cell negatively and makes it difficult to complete a program operation [4, 7, 20, 21, 22]. Thus, the program operation becomes slower while the erase operation becomes faster.

The Fowler-Nordheim equation describing the tunnel current responsible for programming and erasing has a weak temperature dependency. That is an advantage for the performance of flash memory [11]. In addition, atomic silicon diffusion is very low at temperatures less than one-third of the melting point of Si (1414ºC) where not much atomic motion is expected. Thus flash memory operation should be robust for a wide range of temperatures.

Space missions during real-time operation can involve multiple harsh environments necessitating tolerance towards high

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radiation, high endurance and extreme temperature. Thus, understanding failure of flash memories under different stress conditions and their coupled effects is necessary. In this study, we utilize the pulsed programming method as a characterizing technique to investigate the nature and property of trap states present in a single level cell (SLC) NAND. The method described here is applicable to a wide variety of flash NAND memory parts, especially those of SLC architecture. As reported by Roach et al {4, 5, 6], proper program timing is very crucial for the pulsed programming; a pulse width was chosen which is significantly smaller than the timescale of room temperature annealing of the radiation induced traps. We find that after exposure of gamma radiation or total ionizing dose (TID) the program operation requires more pulses. In other words, it takes longer time to program when the amount of ionizing radiation dosage has increased. In addition, as the endurance stress is increased, it takes fewer pulsed programs to program all the bits on one page, thus making the program operation faster. Some blocks were subject to different amount of endurance stress prior to radiation exposure. For those blocks, we found that the programing time of on the cycled NAND also increase with increasing TID radiation doses. The negatively charged electron oxide traps due to cycling and the positively charged hole oxide traps due to TID appear to exhibit a linear-correlation with each other. One possible explanation is the presence of neutral defect centers in the oxide that have the capability of trapping electron or holes and are spatially distributed randomly in the oxide. Aitken et al. [6] first proposed the neutral oxide traps and later many works followed [7, 8, 9] and P. Lenahan and Dressendorfer [10] confirmed the presence of such centers in SiO_2. Oldham et al. [11] also made a similar observation of this neutral oxide traps in his radiation works. Most of the studies that have concluded the presence of neutral oxide traps typically subject the device to radiation exposure prior to the endurance stress. Thus, the holes created due to incoming radiation are mainly responsible for initial step of breaking the weak Si-Si bond, typically near the interface of Si and SiO_2. However, in our combined effects study, the device is subject to radiation exposure post to endurance stress. Under such an experimental condition as well we observe a similar behavior. The lack of sensitivity to the order of stress application suggests that the two types of traps formed may be spatially decoupled. Further studies are necessary and currently in progress.

II. EXPERIMENTAL

A. Sample description and analyzer setup

The samples studied in this article are 1 Gb SLC NAND Flash memories from Micron Semiconductor (Part number MT29F1G08ABAEAWP and lot date code 1652). The chip has a total of 1024 blocks and 64 pages per block. It has 2112 bytes per page. Each page contains a total of 16,896 bits. It requires a typical 3.3 V power supply and has the operation temperature range from -40ºC to 70ºC. The chip has an endurance rating of 10^5 program-erase cycles as stated by the datasheet from the manufacturer [16]. While this is the part chosen for our in-depth study, we have found the pulsed programming method to be generally applicable to NAND parts from a number of vendors.

The chips were characterized via a commercial FPGA-based flash analyzer. A base clock of 50 ns was chosen for all experiments when the daughterboard was directly connected to the motherboard. Prior to performing a single partial program, an "ERASE" command is issued to set all the bits to "1" state. The pulsed programming takes advantage of the fact that a "RESET" command can be issued while the chip is still busy [15]. This partial program is executed in three sequential steps as follows. First, a "PROGRAM" command is issued and executes for a length of time referred to here as pulse-width. Once the predefined time or pulsed-width has elapsed, a "RESET" command is issued to abort the program operation. It is anticipated that the part's internal circuitry managed the "RESET" command and carries the program on to a safe stopping point. We believe this may be where each bit on the selected page has experienced a single program pulse. A "READ" command is issued after that to determine the state of the bits on the selected page.

B. Experimental details

A set of three different experiments were performed which detail the effects of timing, radiation and program-erase stress. Six parts were tested using the FPGA tester. One part was exclusively used for studying the effect of timing on the number of pulsed programs. Different pulse-widths were tried on a particular page to observe the change in the average bit count value of an entire page. A minimum pulse time of 17.5 µs was found to be necessary for a block of NAND bits to be programmed within finite experimental time. However, this minimum pulse time takes about 90 min to program 98 % of the bits. Thus, a more manageable pulse-width of 20 µs was used for all the experiments. Another part was used for radiation testing. Radiation exposure testing with a Co^{60} (1.332 and 1.173MeV gamma) radiation source was conducted at NASA's Jet Propulsion Laboratory Total Ionizing Dose laboratory. All tests and irradiation were performed at room temperature unless otherwise specified. The dose rates were confirmed with air ion chamber measurement.

Four separate blocks of NAND bits were selected on the radiation test chip and they were cycled for 10, 4K, 10K and 25K program-erase cycles, respectively, before the irradiation. This chip was exposed to Co^{60} gamma radiation until it reached a total accumulated ionizing dose levels of 10Krad (Si), 20Krad (Si), 30Krad (Si), 50Krad (Si) and 75Krad (Si). At each TID level, the designated test blocks were examined using the pulsed programming technique to study the impact of the TID radiation.

III. RESULTS

NAND Flash devices use incremental step pulse programming to achieve fast program performance and a tight threshold voltage distribution [28]. The ISPP typically starts off with an initial program pulse (~ 15 V, which is followed by incremental pulses (~0.5-1.0 V) which reach a maximum value (~20 V) [27]. By using incremental step pulses, a higher voltage is reached without increasing the programming time [28]. Thus, the timing is crucial to partial page programming. Different pulse-widths were used to completely program a page using partial programming method. The summary of the results is show in Fig. 1, where the pulse-width is shown in units of programming time t_{PROG} = 200 µs [16]. As expected, as the pulse-width increases, the number of pulses needed to program all 16896 bits on the page decreases. A pulse width of 16 µs or lesser was never able to program a single bit on the page even after several (100 K) pulses. This suggests that the internal charge pumps might not reach the initial programming voltage (~15 V). However, the partial programming with pulsed width

of 17.5 µs took excessively long (~3 hours) to execute. Whereas, increasing the pulse width by ~10% to 20 µs resulted in an 8x reduction in execution time to completely program all the 16896 bits on the selected page. Pulse widths of 22.5, 25 and 50 all fall on the same curve suggesting internal safety features completed the same cycle of programming for all bits regardless of pulse width within that range. Thus, all the partial programs in this study are executed with a pulse-width of 20 µs as the smallest pulse width supportable by this study to give the definition between bits. As the number of pulsed-programs increases, the programmed bits distribution shifts towards "0" state from "1" state and eventually all the bits are programmed to "0" [4, 5, 6].

Total ionization dose and Program-Erase stress

The results of TID and program erase cycling stress are summarized in Fig. 2 and Fig. 3, respectively. To observe the effect of program-erase stress, partial programming was performed on the same page after reaching the desired program-erase stress cycles. The same chip was then irradiated with a Co^{60} source until it reached the total accumulated target dose, then a pulsed program characterization was performed. Fig. 2 shows the individual effect of program/erase stress and TID stress separately on the pulsed programming behavior of the NAND chip. Consistent with the findings of Roach et al, TID decreases program speed and program/erase cycling stress increases it [4].

Fig. 3 summarizes the coupled effects of program-erase stress and radiation induced damage. Each plot shows the partial programming behavior of the selected pages where each page underwent 10, 4K, 10K, 25K program-erase cycles and irradiated with a series of TID doses from 0krad to 75krad. The results showed the increasing program-erase stress effectively speeds up the programming time (equivalent to fewer number of program pulses needed). As the TID doses increases, the NAND chip slows down (equivalent to higher number of program pulses needed). These general observations are independent of the TID doses which is summarized in Fig. 4. As shown in Fig. 4 the number of pulsed-programs needed to program 50 % of the bits on the page is plotted against the number of program-erase cycles. It can be seen that as the endurance stress increases, the number of pulsed programs decreases. Opposite effect is observed for TID, as the dose increases the pulsed programs also increases.

Bit-distribution and Logistic model

During the "READ" operation in a pulsed-program the logical addresses of all 16896 bits present on a Page were recorded. After every pulsed-program was issued the logical bit-address and bit-value of that particular bit was recorded through-out the entire sequence until the all the bits in the entire Page are in programmed state. Each logical bit-address is then associated with the pulsed-program where it switches from 1 to 0. The normalized distribution of these pulsed-programs is plotted in Fig. 5 where the shape of the distribution fits well with a logistic growth model [29, 30] as shown in Fig 6 where the goodness of fit R-square is 0.99.

Logistic growth/decay model is governed by growth/decay dependent on availability of resources and maximum capability sustainable by the environment, often called as carrying capacity [29, 30]. For the pulse-programming data, the maximum carrying capacity in the logistic growth model is the fixed total number of bits (16896). The logistic growth/decay model equation is given by

$$y = \frac{1}{1+e^{a(x-b)}},$$

Where "a" is the slope of the growth or decay i.e. the growth or decay rate, "b" is 50% inflection point.

Fig. 7 illustrates the goodness of fit using the logistic growth model for pulse-programming of pages that were subjected to different levels of endurance stress. All the fits have R-squared value of about 0.9. The fit parameters, "a" and "b", slope and inflection point are shown in Fig. 8 and plotted as a function of program-erase cycles. Experimentally, we observe that the slope "a" is not a strong function of program-erase cycles while the inflection point "b" decreases monotonically with respect to program-erase cycles. A constant 'a" suggests the memory bits in the selected page responds uniformly to the programming pulses. The decreasing "b" indicates the response of the memory bit distribution towards the increasing charged oxide traps density in the tunnel oxide. These parameters can be used to quantify the pulsed-program behavior of the SLC NAND chips.

IV. DISCUSSION AND CONCLUSION

From Fig. 2, it can be clearly seen that as the TID is increased it takes longer to fully program the page and as the program-erase stress is increase it becomes easier to program a particular page for the range of TID undertaken in this experiment. This behavior was also previously observed and consistent with the nature of the traps known to be introduced by these two effects individually [7]. The TID introduces an electron-hole pair in the oxide and under external field such as those applied during read and programming, the electron is swept away [7]. However, the hole transports towards the Si/SiO_2 interface and have a higher probability to be trapped. TID creates a positive oxide trap state and thus, requires a larger potential during a program operation to overcome this barrier and introduce a charge in the floating gate.

In the case of program-erase stress, electrons injected into the oxide can be trapped by the neutral oxide trap and create a negatively charged trap. This excess charge is interpreted as a stored charge in floating gate during a read operation and thus the programming is faster after a block has experienced a large program-erase stress.

In our experiments, we explore the couple effect of these two trap states. We observe that the positive-hole and negative-electron traps states appear to be coexistent without non-linear interactions based on the responses of the SLC NAND chips towards the endurance cycling and TID exposures. We postulate that the negative-electron traps, as a result of program-erase cycling, and the positive-hole traps, due to TID, are physically located in different regions in the tunnel oxide. The bulk of the oxide and the positive-trap state can be located near the interface. Since, we do not radiate the chips prior to program–erase cycling, a trap state created due to an incoming hole from the radiation as proposed, might not be fully applicable [8]. Fig. 4 clearly displays the opposing effects of TID and endurance stress. One can expect that the opposite effects can cancel each other out. From the first glance it does appear that the damage

done by TID can be neutralized by subjecting the chip to an appropriate endurance stress. However, if endurance does recover the damage from TID the data retention of such a sector should be significantly similar to the chip before any irradiation. Data retention on a chip which was irradiated up to 75 Krad (unbiased with all pins grounded) and was subject to 25K pre-radiation program-erase cycles, successfully retained the data for up to 1 week at 100ºC. Also, another chip was exposed to irradiated to 25 Krad (Si) (biased at 3.6 V) and which also retained data with no errors, both at room temperature and at 150ºC. Such an observation was previously seen in different NAND Flash chips as well with respect to the room temperature studies [19, 3]. The oxide traps induced by radiation and P/E cycling exhibit independent behaviors.

The physical location of these oxide traps plays a significant role in such experiments. The radiation can induce positive oxide traps at three different locations: viz. near the interface of Si/SiO_2 [26, 27], in the bulk oxide [26. 27] and in the shallow trench isolation (STI) oxide [17]. The P/E cycling can induce negative traps in the bulk oxide and the interface traps at the Si/SiO_2 interfacial layers [18]. The neutral oxide trap states can accommodate both the positive trap (Radiation induced) and negative trap (P/E cycling) present in the bulk oxide or near the interface of Si/SiO_2. However, the positive traps in the STI oxide could still have pronounced effect on the device performance [17]. A better understanding of the effect of physical location of oxide traps could help to decouple the radiation and P/E cycling induced effects and further our understanding

In conclusion, we are able to successfully utilize partial-page programming as a chip level characterizing technique to investigate NAND degradation mechanism at the memory bit level. We also illustrate that a logistic distribution model can fit the pulse-programming data and extract quantifiable fitting parameters to correlate the memory bits with uniformity (slope "a") and programming behavior (inflection points "b"). This technique can be useful to study the NAND flash memory at the chip level.

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Figure 1: Effect of interrupt time on partial page programming curve in units of programming time (t_{PROG} = 200 µs)

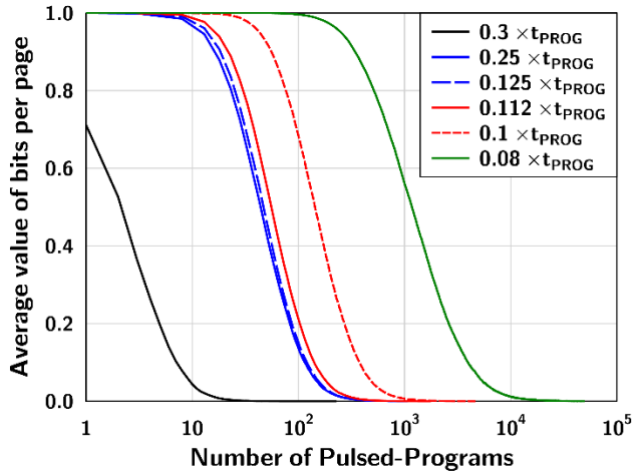

Figure 2: Effect of total ionizing dose and program-erase stress individually on partial page programming

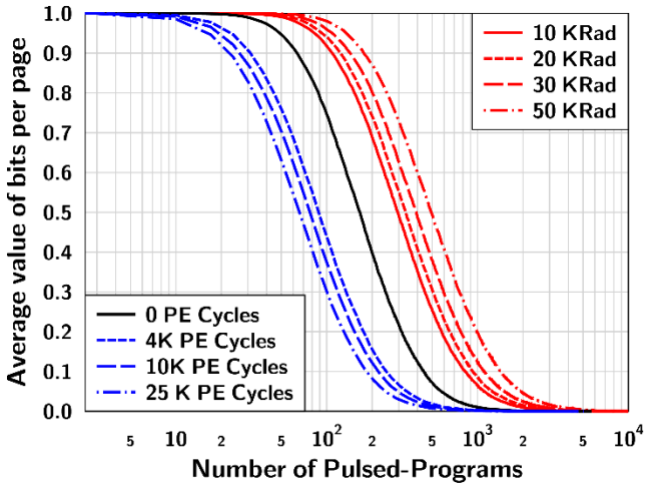

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Figure 3: Coupled effect of TID and program-erase stress on partial page programming

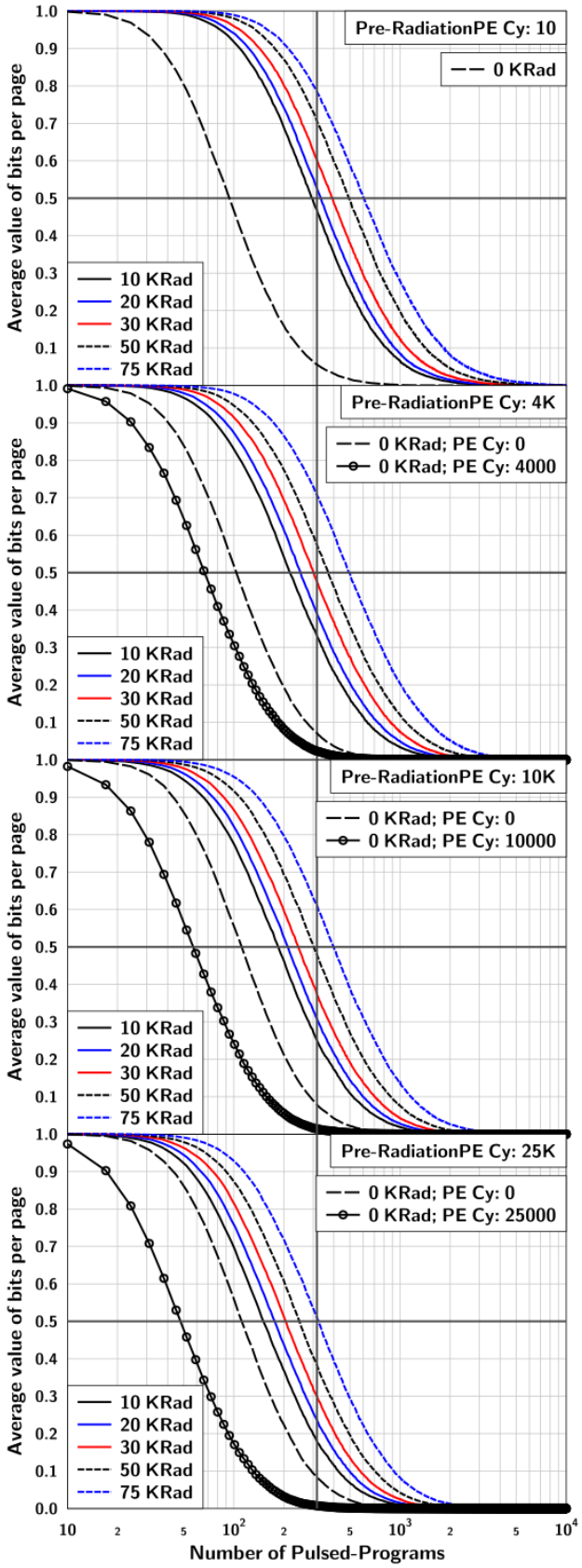

Figure 4: Number of pulsed programs needed for TID and endurance stress.

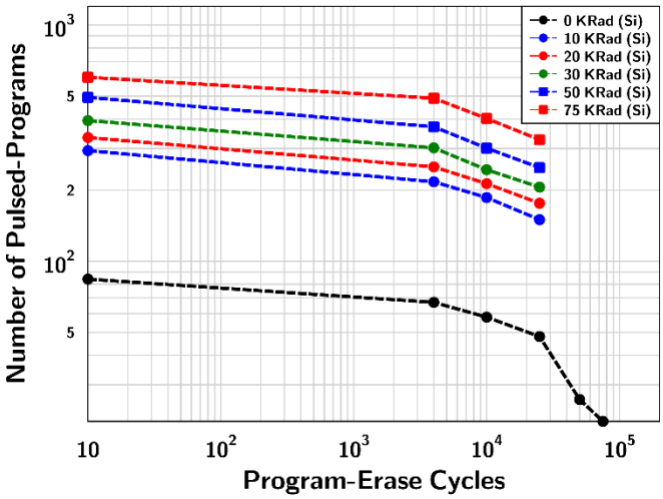

Figure 5: Bit distribution of programmed bits during a pulse-programming of a Page with zero program-erase cycles.

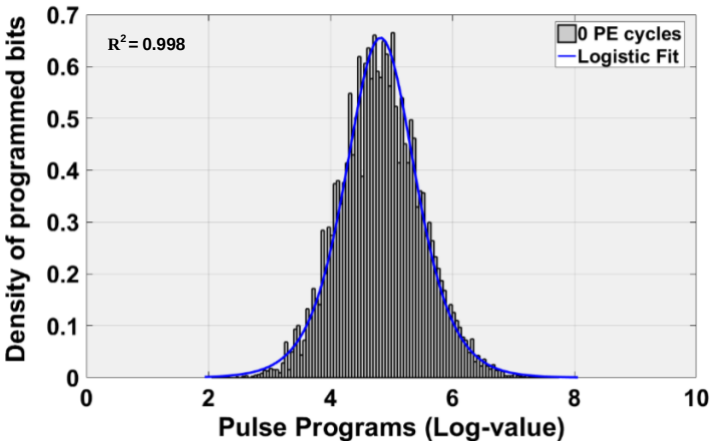

Figure 6: Logistic fit to pulse-programming of a Page with zero program-erase cycles

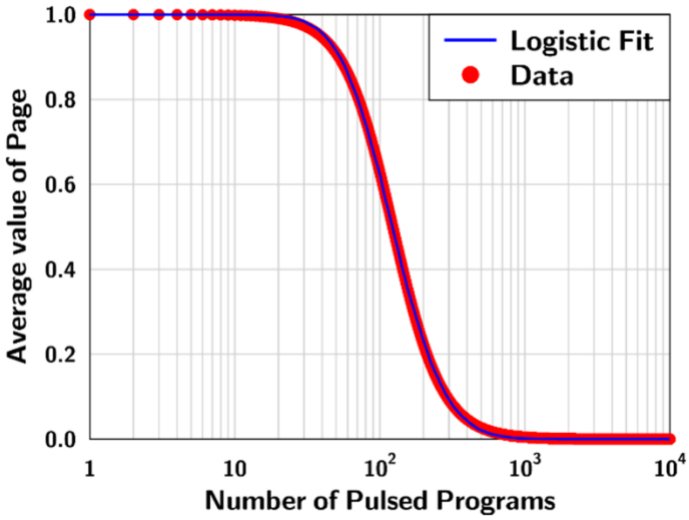

Figure 7: Logistic fit to pulse-programming of a Page with various levels of endurance stress

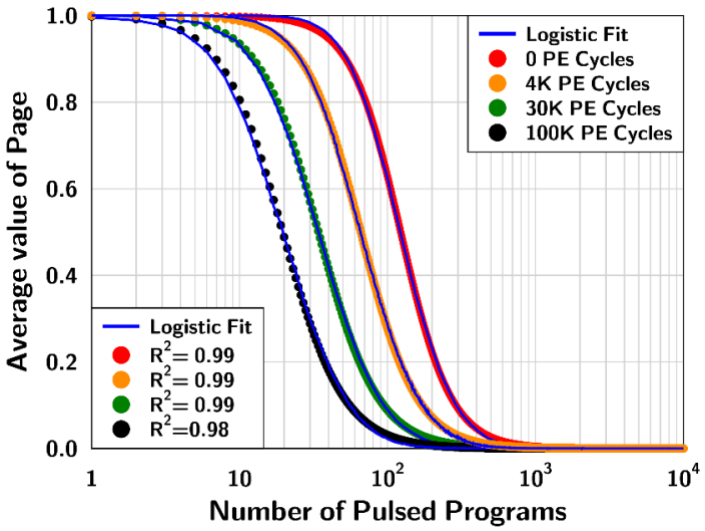

Figure 8: Parameters of Logistic fit to pulse-programming of a Page vs program-erase cycles